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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER

KING, JUSTIN

ART UNIT	PAPER NUMBER
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2111

DATE MAILED: 09/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/933,547

Applicant(s)

HUNSAKER, MIKAL C.

Examiner

Justin I. King

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 July 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-29 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3, 8-13, 18-23, 28 and 29 is/are rejected.
- 7) ☒ Claim(s) 4-7, 14-17 and 24-27 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 7/1/04 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Klein (U.S. Patent No. 6,047,349).

Referring to claims 1 and 11: Klein discloses an apparatus (structure 106 in figure 4) comprising an input circuit (structure 106's portion connecting to the PCI bus, structure 122 in figure 5) coupled to a first bus (the PCI bus) to transfer a transaction data having a transaction identifier (the PCI packet address) to one of N buffers (structure 108 in figure 4). Since the delay transaction (DT) is an inherent PCI protocol behavior (Application, page 1), Klein's data transaction is a delayed transaction. Klein further discloses an output circuit (figure 5, structure 120) coupled to the buffers to transfer the DT data from the one of the N buffers to a second bus operating at the bus frequency. Since the input circuit is connecting to the PCI bus, output circuit is connecting to the CPU bus, and the controller (106) has the memory for buffering the PCI delay transaction, and each data transmission will allocate dynamically the necessary buffer due to the difference in the bus frequencies; the input and output circuits cooperate with the buffer controlling means to accommodate the data transmission from different bus frequencies;

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hence, the circuit is dynamically configured based on the bus frequency, and claims are anticipated by Klein.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-3, 8-10, 11-13, and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lange (U.S. Patent No. 5,941,970) in view of Murdoch et al. (U.S. Patent No. 5,857,082).

Referring to claim 1: Lange discloses an apparatus (figure 4) comprising an input circuit (structure 206 in figure 4) coupled to a first bus to transfer a PCI transaction data, which is a delay transaction, having a retry register coupled to memory queue to re-enter the commands that are not completed successfully (column 3, paragraph 3). Since Lange discloses tracking the incomplete commands and enters the command into the buffer (structures 248 and 246 in figure

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4), Lange discloses that one of the buffers associated with the transaction identifier. Lange further discloses an output circuit (structure 208 in figure 4) coupled to the buffers to transfer the DT data from the one of the N buffers to a second bus. Although Lange discloses that the apparatus is applicable to many digital communication environments (column 4, lines 33-34), Lange does not explicitly disclose that the apparatus will dynamically configured according to the attached bus' frequencies. Murdoch discloses that it is known to use the buffer to transmit data between buses with different frequencies (abstract). Since each data transmission will allocate the necessary buffer due to the difference in the bus frequencies, the input and output circuits cooperate with the buffer controlling means to accommodate the data transmission from different bus frequencies; hence, the circuit is dynamically configured based on the bus frequency. Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Murdoch's teaching onto Lange because Murdoch teaches one to manage the latency between different bus frequency/speed.

Referring to claim 2: Lange discloses a PCIM (figure 4, structure 242) to transfer the retry command into one of the buffers. Lange's PCIM is the decoder, which is a 1-to-N demultiplexing circuit to transfer the DT data from the first bus to the one of the N buffers based on the transaction identifier.

Referring to claim 3: Lange discloses the apparatus wherein the output circuit comprises a N-to-1 multiplexing circuit to transfer the DT data from the one of the N buffers to the second bus based on the transaction identifier (column 3, paragraph 3).

Referring to claim 8: Lange discloses a primary bus (figure 1, host bus) and a memory (structure 12, figure 1).

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Referring to claim 9: Lange discloses a PCI bus (figures 1 and 3-4).

Referring to claim 10: The delay transaction is PCI's inherent behavior and the split transaction is PCI-X's inherent behavior. PCI-X is an extension of the PCI bus protocol.

Referring to claim 11: Lange discloses an apparatus (figure 4) comprising an input circuit (structure 206 in figure 4) coupled to a first bus to transfer a PCI transaction data, which is a delay transaction, having a retry register coupled to memory queue to re-enter the commands that are not completed successfully (column 3, paragraph 3). Since Lange discloses tracking the incomplete commands and enters the command into the buffer (structures 248 and 246 in figure 4), Lange discloses that one of the buffers associated with the transaction identifier. Lange further discloses an output circuit (structure 208 in figure 4) coupled to the buffers to transfer the DT data from the one of the N buffers to a second bus. Although Lange discloses that the apparatus is applicable to many digital communication environments (column 4, lines 33-34), Lange does not explicitly disclose that the apparatus will dynamically configured according to the attached bus' frequencies. Murdoch discloses that it is known to use the buffer to transmit data between buses with different frequencies (abstract). Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Murdoch's teaching onto Lange because Murdoch teaches one to manage the latency between different bus frequency/speed.

Referring to claim 12: Lange discloses a PCIM (figure 4, structure 242) to transfer the retry command into one of the buffers. Lange's PCIM is the decoder, which is a 1-to-N demultiplexing circuit to transfer the DT data from the first bus to the one of the N buffers based on the transaction identifier.

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Referring to claim 13: Lange discloses the apparatus wherein the output circuit comprises a N-to-1 multiplexing circuit to transfer the DT data from the one of the N buffers to the second bus based on the transaction identifier (column 3, paragraph 3).

Referring to claim 18: Lange discloses a primary bus (figure 1, host bus) and a memory (structure 12, figure 1).

Referring to claim 19: Lange discloses a PCI bus (figures 1 and 3-4).

Referring to claim 20: The delay transaction is PCI's inherent behavior and the split transaction is PCI-X's inherent behavior (Specification, page 1). PCI-X is an extension of the PCI bus protocol.

6. Claims 21-23 and 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Klein, Lange, and Murdoch.

Referring to claim 21: Klein discloses a processor (figure 4, structure 102) having a host bus (figure 4, structure CPU bus), a memory (figure 4, structure 108) having a first bus (figure 4, the combined structure 110 and 112), and chipset (figure 4, structure 106) coupled to the processor via the host bus and to the memory via the first bus, to control access to the memory from a device via a second bus (figure 4, structure 116). Klein's chipset does not explicitly disclose buffer circuits.

Lange discloses an apparatus (figure 4) comprising an input circuit (structure 206 in figure 4) coupled to a first bus to transfer a PCI transaction data, which is a delay transaction, having a retry register coupled to memory queue to re-enter the commands that are not completed successfully (column 3, paragraph 3). Since Lange discloses tracking the incomplete

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commands and enters the command into the buffer (structures 248 and 246 in figure 4), Lange discloses that one of the buffers associated with the transaction identifier. Lange further discloses an output circuit (structure 208 in figure 4) coupled to the buffers to transfer the DT data from the one of the N buffers to a second bus. Although Lange discloses that the apparatus is applicable to many digital communication environments (column 4, lines 33-34), Lange does not explicitly disclose that the apparatus will dynamically configured according to the attached bus' frequencies. Murdoch discloses that it is known to use the buffer to transmit data between buses with different frequencies (abstract).

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Lange and Murdoch's teaching onto Klein because Murdoch teaches one to manage the latency between different bus frequency/speed and Lange teaches one to provide high data throughput across a bus bridge, while efficiently effectuating the data transfer by optimizing the use of data register space and design flexibility (Lange, column 2, lines 58-60).

Referring to claim 22: Lange discloses a PCIM (figure 4, structure 242) to transfer the retry command into one of the buffers. Lange's PCIM is the decoder, which is a 1-to-N demultiplexing circuit to transfer the DT data from the first bus to the one of the N buffers based on the transaction identifier.

Referring to claim 23: Lange discloses the apparatus wherein the output circuit comprises a N-to-1 multiplexing circuit to transfer the DT data from the one of the N buffers to the second bus based on the transaction identifier (column 3, paragraph 3).

Referring to claim 28: Lange discloses a PCI bus (figures 1 and 3-4).

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Referring to claim 29: The delay transaction is PCI's inherent behavior and the split transaction is PCI-X's inherent behavior (Specification, page 1). PCI-X is an extension of the PCI bus protocol.

Response to Arguments

7. In response to Applicant's argument that Klein does not expressly or inherently disclose a delayed transaction (Remark, page 12, lines 4-5): Klein does inherently disclose the delayed transaction. As stated in the Application page 1, the delayed transaction is a part of the PCI protocol behavior. Since Klein discloses the PCI bus, thus, Klein does inherently discloses the PCI's delayed transaction.

8. In response to Applicant's argument that Klein does not disclose the input circuit and output circuit dynamically configured according to a bus frequency, and the Klein does not disclose the output circuit transferring the DT data to a second bus (Remark, page 12, lines 5-7, page 12, lines 10-12): The claim language is interpreted as broad as possible during examining process. The claim language merely claims the circuits configured according to the bus frequency. Klein's circuits transfer data from two separate buses (PCI bus and CPU bus) with different bus frequencies. Klein discloses RAM (figure 4, structure 108) for buffering the data transmission between those two buses. Since each data transmission will allocate the necessary buffer due to the difference in the bus frequencies, the input and output circuits cooperate with the buffer controlling means to accommodate the data transmission from different bus frequencies; hence, the circuit is dynamically configured based on the bus frequency.

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9. In response to Applicant's argument that Klein only discloses a memory to store data, not DT data (Remark, page 12, line 9): As stated in the specification, the DT is an inherent PCI protocol behavior, and Klein discloses a PCI bus. Thus, Klein discloses the DT data.

10. In response to Applicant's argument that Lange does not disclose delayed transaction (Remark, page 14, line 6) and Lange's bus interface does not dynamically configured according to a bus frequency (Remark, page 14, lines 6-7): As stated in the specification, the DT is an inherent PCI protocol behavior, and Lange discloses a PCI bus. Thus, Lange discloses the DT. As the rejection states, Lange's interface does not dynamically configured according to the bus frequency, and Murdoch discloses that it is known to use the buffer to transmit data between buses with different frequencies (abstract). Since each data transmission will allocate the necessary buffer due to the difference in the bus frequencies, the input and output circuits cooperate with the buffer controlling means to accommodate the data transmission from different bus frequencies; hence, the circuit is dynamically configured based on the bus frequency. Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Murdoch's teaching onto Lange because Murdoch teaches one to manage the latency between different bus frequency/speed.

11. In response to Applicant's argument that Murdoch does not disclose dynamically configuration according to the bus frequency (Remark, page 14, lines 7-9): Murdoch discloses that it is known to use the buffer to transmit data between buses with different frequencies (abstract). The dynamically buffer allocation for each data transmission is the dynamically configuration.

Allowable Subject Matter

12. Claims 4-7, 14-17, and 24-27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. The following is a statement of reasons for the indication of allowable subject matter: The prior arts on record do not explicitly disclose a bus bridge with the claimed structure to manage the buffer and to support the dynamically configuring I/O circuits according to the bus frequency.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin I. King whose telephone number is 703-305-4571. The examiner can normally be reached on Monday through Friday, 9:00 am to 5:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-308-3110. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

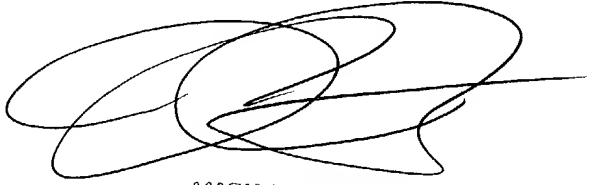
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at <http://www.uspto.gov/ebc/index.html> or 1-866-217-9197 for information on this policy. Requests to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.



Justin King
September 2, 2004



MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100